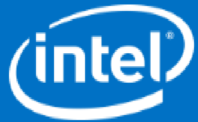
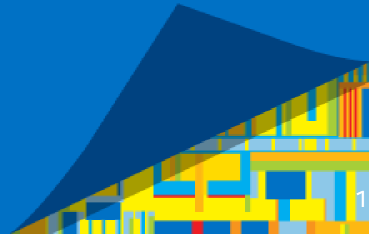


DOE Lab Opportunities to Enable Moore's Law

Janice Golda

Director, Lithography Strategic Sourcing

Global Supply Management



Predictable Silicon Track Record

Executing to Moore's Law

Enabling new devices with higher functionality and complexity while controlling power, cost, and size

Strained Silicon

Hi-K Metal Gate

3D Transistors

90 nm | 65 nm | 45 nm | 32 nm | 22 nm | 14 nm | 10 nm | 7 nm

LEADING EDGE PROCESS TECHNOLOGY

Transistor Performance/ Generation

Energy

Moore's Law Virtuous Circle: Enabling HPC

The Most Advanced Supercomputer Ever Built

An Intel-led collaboration with ANL and Cray to accelerate discovery & innovation

Argonne NATIONAL LABORATORY

intel

Prime Contractor

CRAY

Subcontractor

>180 PFLOPS
(option to increase up to 450 PF)

>50,000 nodes

13MW

2018 delivery

18X higher performance†

>6X more energy efficient†

Source: Argonne National Laboratory and Intel.
†Comparison of theoretical peak double precision FLOPS and power consumption to ANL's largest current system, MIRA (10PFs and 4.8MW)

Aurora | *Science From Day One!*

Extreme performance for a broad range of compute and data-centric workloads

Focus Areas

Transportation

Aerodynamics

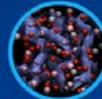
Biological Science

Biofuels / Disease Control

Renewable Energy

Wind Turbine Design / Placement

Materials Science



Batteries / Solar Panels

Computer Science

New Programming Models

Training

Argonne Training Program on Extreme-Scale Computing

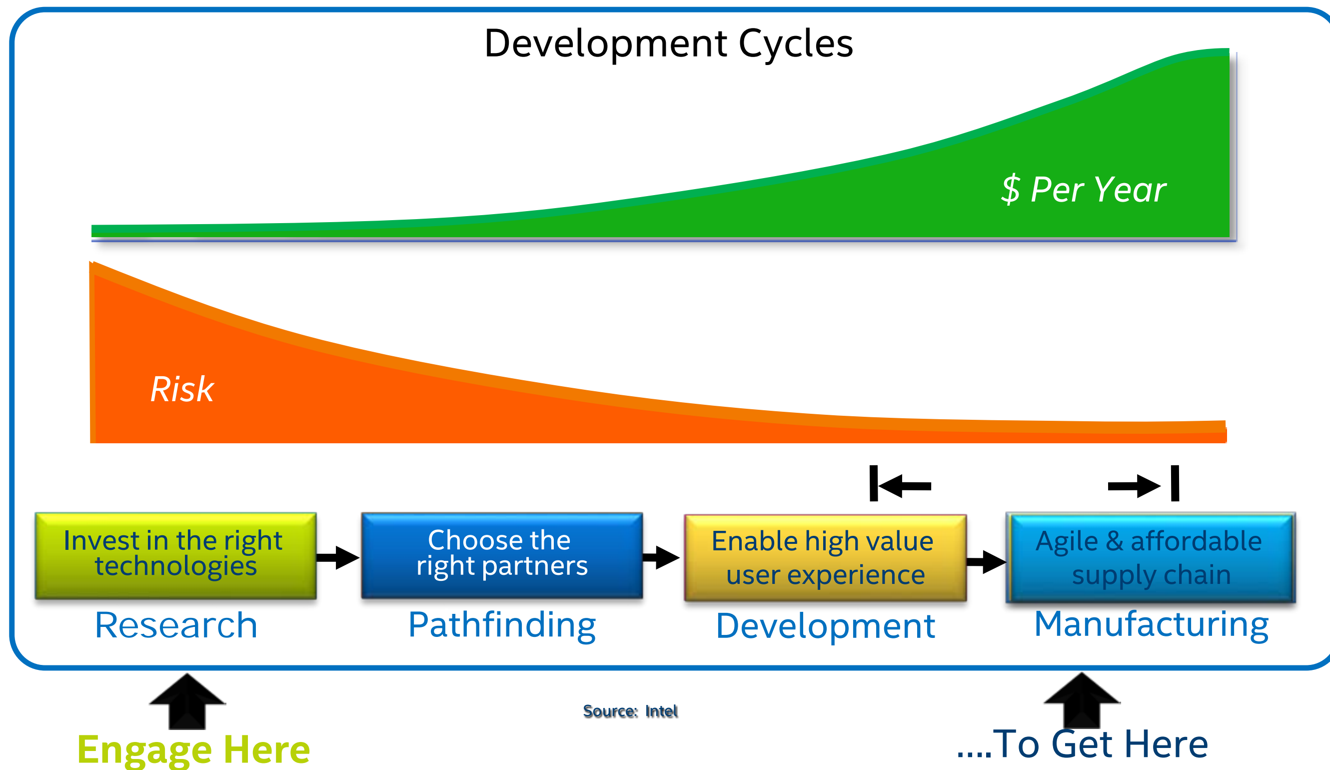
Public Access

US Industry and International

4

Innovation Pipeline to Continue Moore's Law

Shared risk/reward with ecosystem partners



DOE History of Demonstrating Litho Capability

POC essential for disruptive technologies

17

LLNL signs CRADA with 3 US companies

tsmc
TSMC Property

FRIDAY'S Newsline

Published twice weekly for employees of the University of California Lawrence Livermore National Laboratory — Friday, October 16, 1992 — Vol.17 No. 76

Watkins signs LLNL's largest CRADA

By Steve Wampler

Secretary of Energy James Watkins joined representatives from the Laboratory and three California firms yesterday to announce a collaborative research pact that may lead to important advances in manufacturing microelectronic components.

Such advances would permit manufacturing computer chips that are 10 times faster and contain 1,000 times more memory than today's chips, reported Lab scientists.

The four-year Collaborative Research and Development Agreement (CRADA) between the Laboratory and the three electronics companies was signed at the National Technology Initiative conference at the Santa Clara Convention Center.

Valued at $25.2 million, the new CRADA is the largest signed by the Laboratory to work with U.S. businesses to develop new technologies.

This agreement is part of a broader national program in soft

Photo by Bryan …

Energy Secretary James Watkins, center, congratulates Lab scie… Andy Hawryluk, right, and Nat Ceglio on research he described … "concrete evidence of the success of National Technology Initia… Watkins said NTI is "helping U.S. companies leapfrog to next ge… tion technology."

Images courtesy of Nat Ceglio

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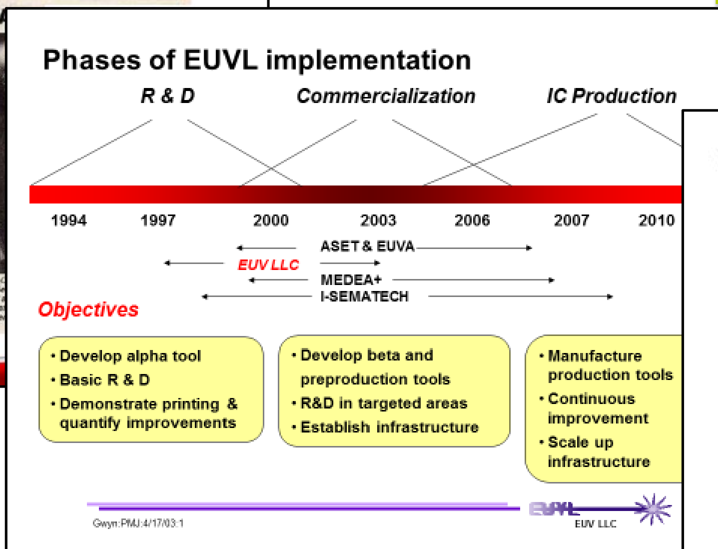


Modules integrated into demonstration alpha tool

Reticle Stage

Engineering Test Stand

Laser Plasma Source

PO Box

Condenser Optic

Wafer Stage

Environment Control

Control & Data Acquisition

Gwyn:PMJ:4/17/03:1

EUV LLC

Originally from Sivakumar, 2013 International Workshop on EUV Lithography

As graded by M. Phillips for 2014 SPIE AL

The Challenges of EUV

Resists

Patterning requirements…

Resolution – On track

LWR/Dose – Need high power

Outgassing- *Testing issues slow development*

IDM TPT requirements

Scanner outgassing requirements

Tool

Source

Availability - *Critical*

Power - *Critical*

Scanner Hardware - On track

Reticle

Defectivity

Killer defect impact >> wafer process defect impact – *need pellicle*

Mitigation strategies

Reticle inspection – *A-PI late, sources for A-PI, AIMS, A-BI are inadequate*

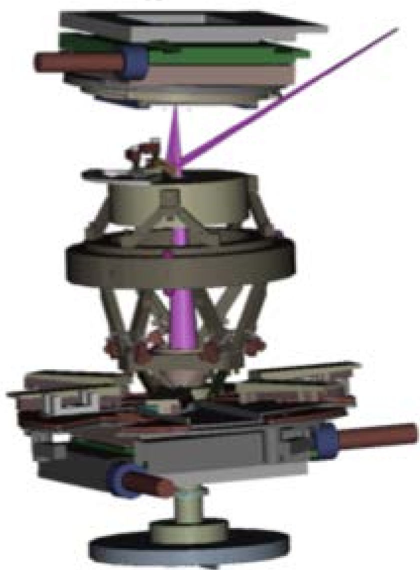
Patterned wafer inspection – *not a substitute for A-PI or pellicle in HVM*

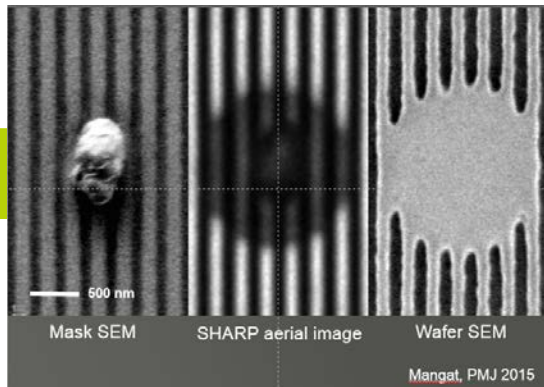
Alternative strategies

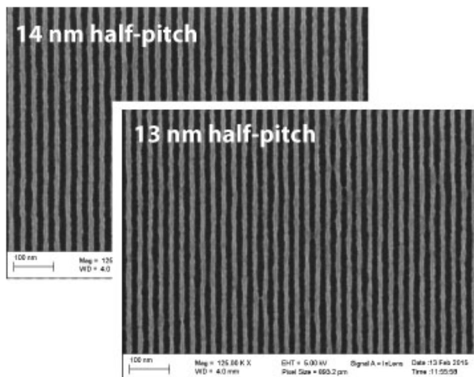
EUV HVM implementation depends on satisfactory progress on all these fronts!

CXRO Provides Unique EUV Capability to Intel

MET





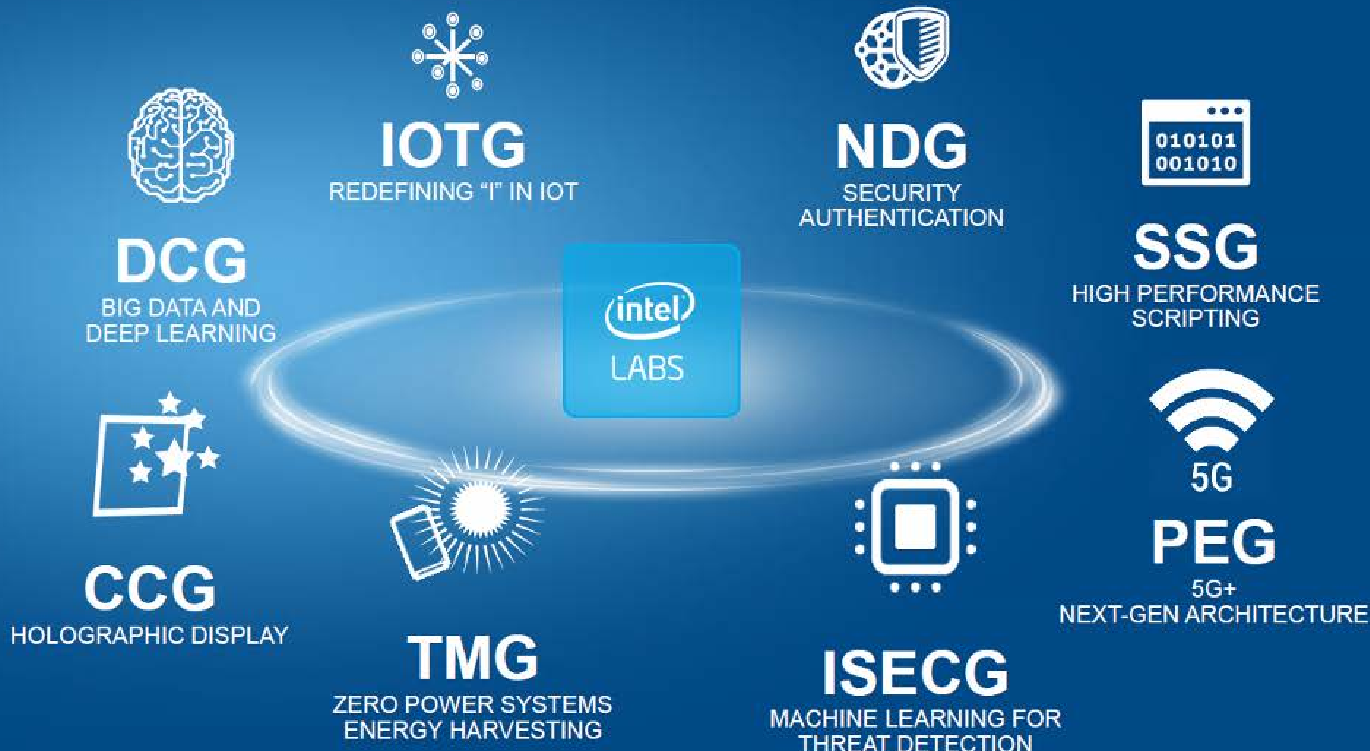


SHARP
SEMICONDUCTOR HIGH-NA ACTINIC RETICLE REVIEW PROJECT

intel

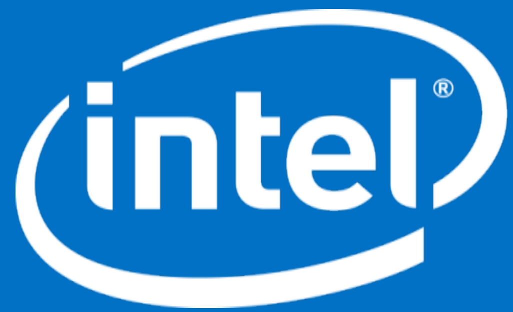
INTEL LABS TOP COLLABORATIVE PROJECTS

Focused collaborations on highest-priority needs for each Intel BU



Going Forward – Collaboration Opportunities

- Enable EUV extension
  - Complete LBNL MET 0.5NA tool upgrade including lens and body + related hardware
  - Continue to expand SHARP tool capability
- Enable early learning in
  - Metrology
  - Nanomaterials characterization
  - Functional imaging



GSM
Global Supply Management