Energy Efficient Electronics

System Challenges & Opportunities

Shekhar Borkar

Intel Corp

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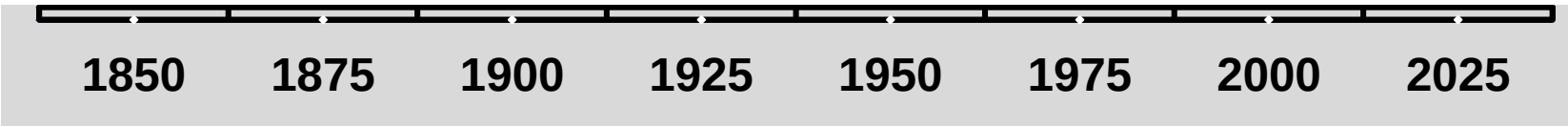
Evolution of Electronics



Mechanical

Electro-Mechanical

Electronic-VT

Bipolar

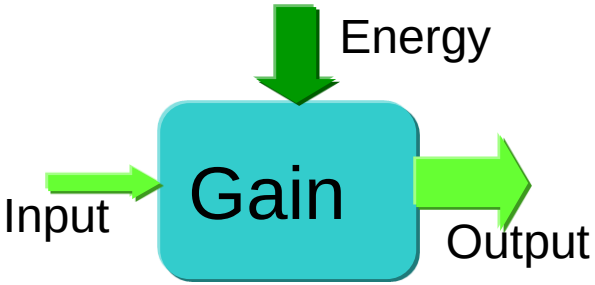
NMOS

CMOS…….⇨ ?

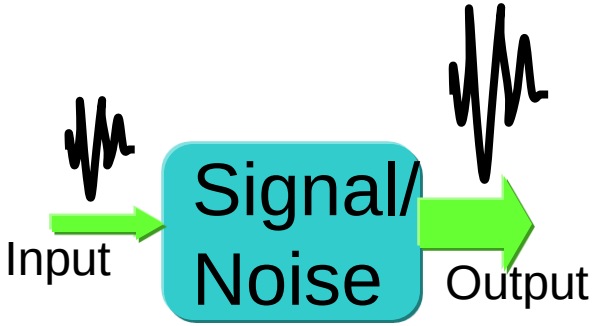
All cross-road technologies show
1. Gain
2. Signal/Noise
3. Scalability

Performance
Energy
Price/Performance

The Three (+ 1) Tenets



(1)



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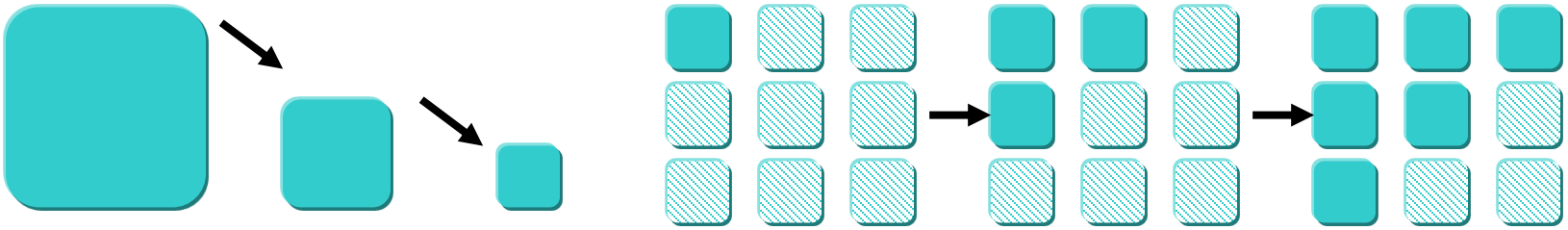
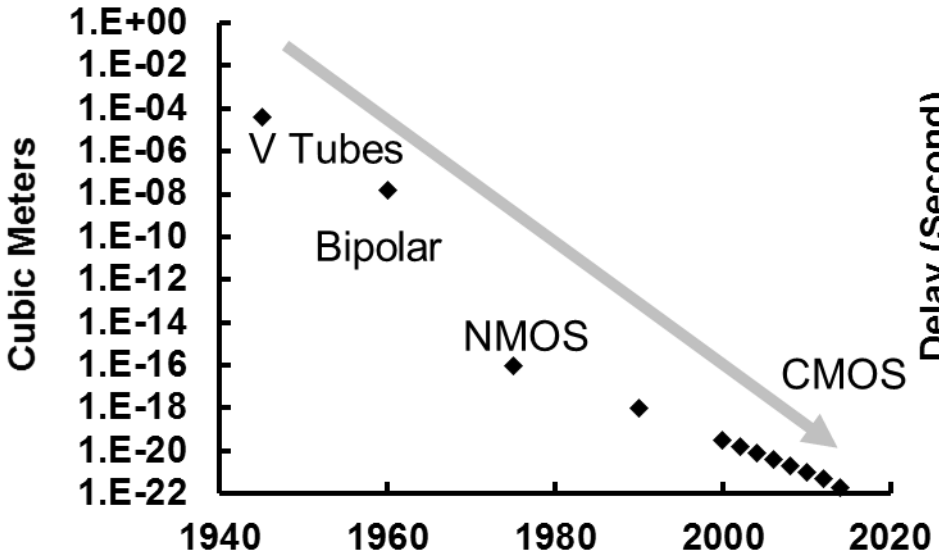


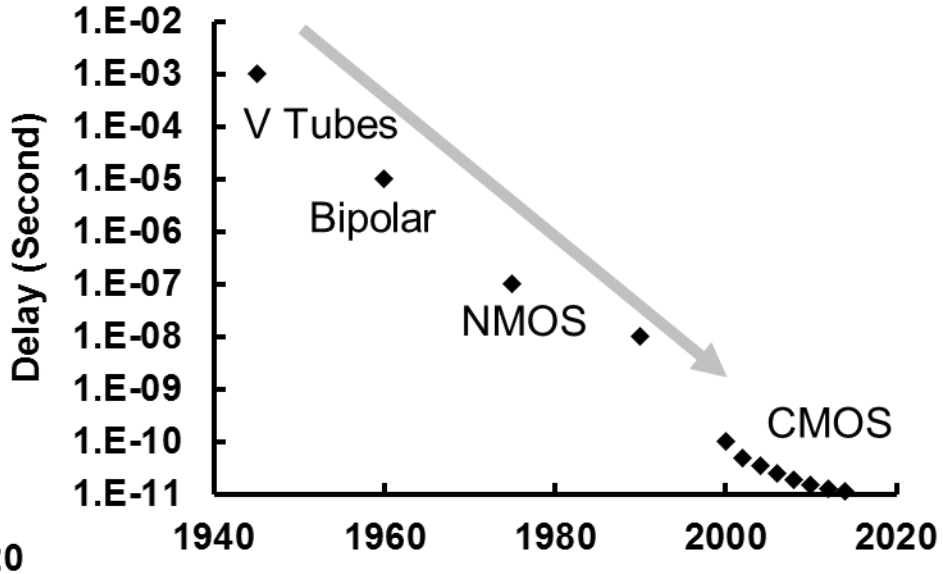
Scalability, in some shape or form

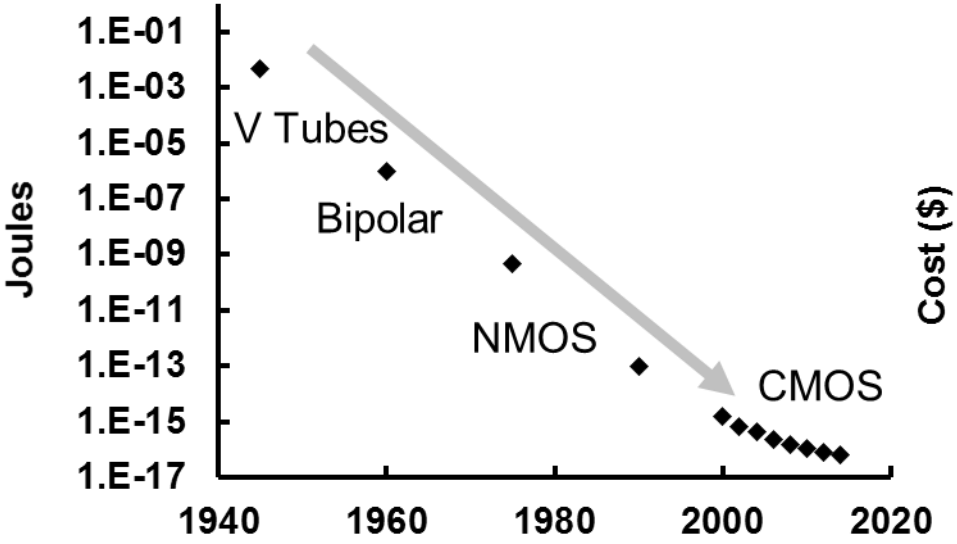
(3)

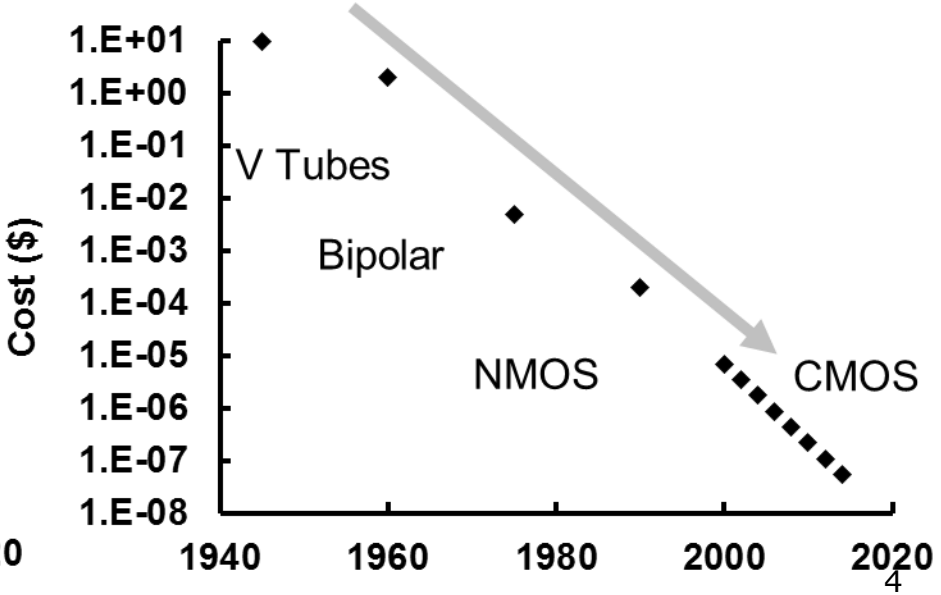
Shalf's tenet: High volume manufacturability (4)

Benefits over Decades









What's in sight after CMOS?

- **Which technology shows gain?**
- **Satisfactory signal to noise ratio?**
  - At room temperature?
- **Scalability in some shape or form?**
  - Performance, Energy, Cost
- **Research must continue to find one**
- **Then it will take 10-15 years to mature**
- **Until then…**

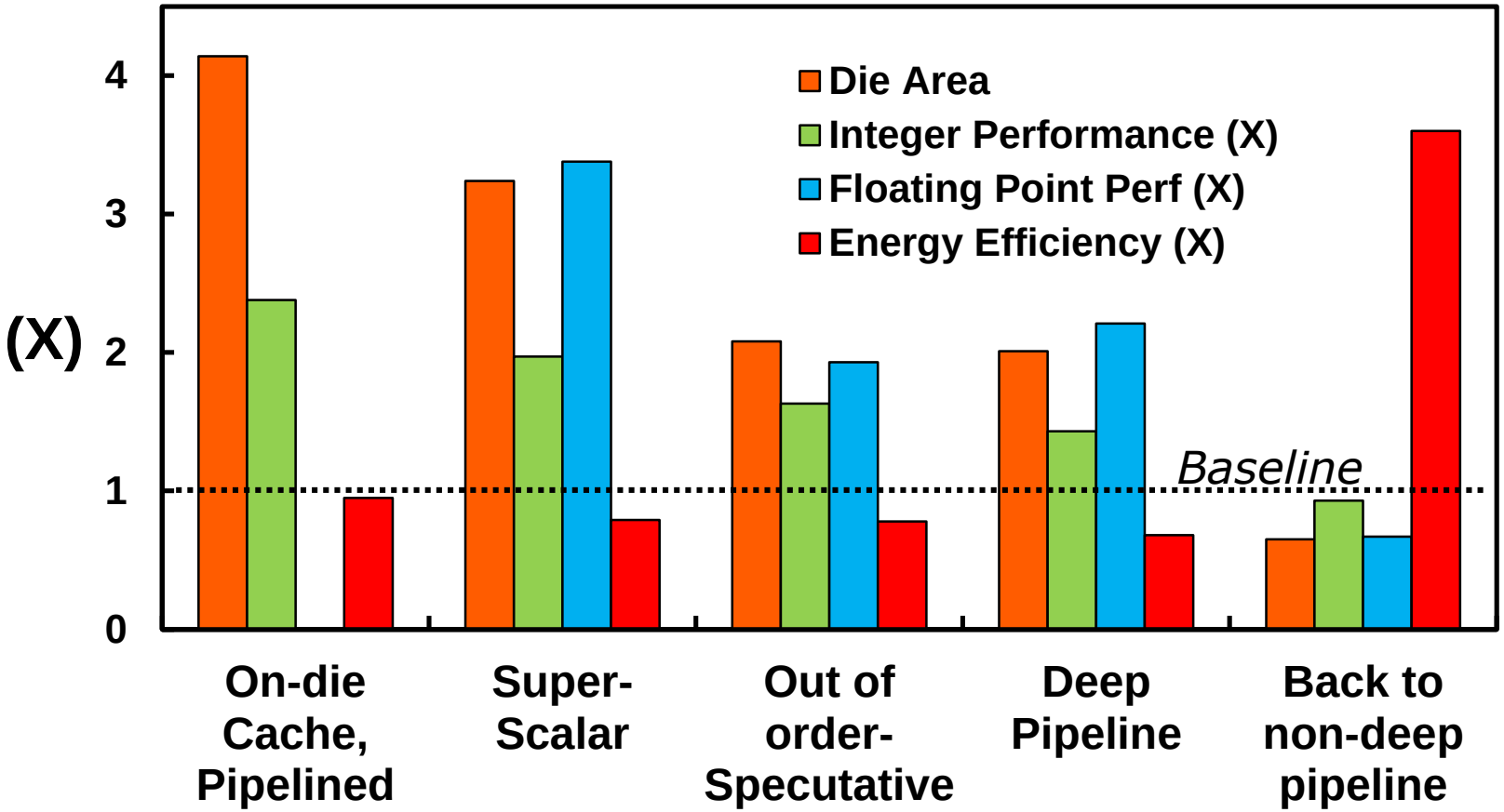
…CMOS must continue

Three Prong Approach

1. Remove waste, reclaim efficiency
2. Employ known techniques

   (which you were afraid to…)
3. Multi-disciplinary approach

Inefficiency in Microarchitectures



Reclaim efficiency with multi—

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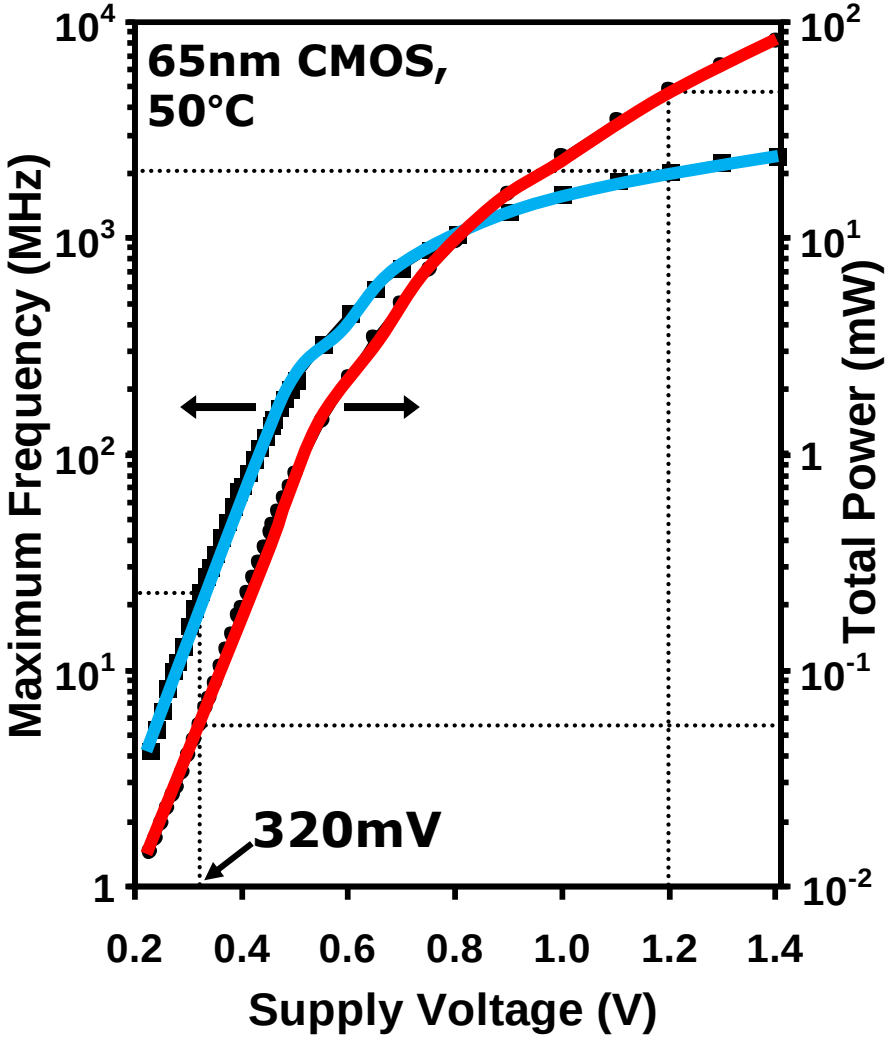
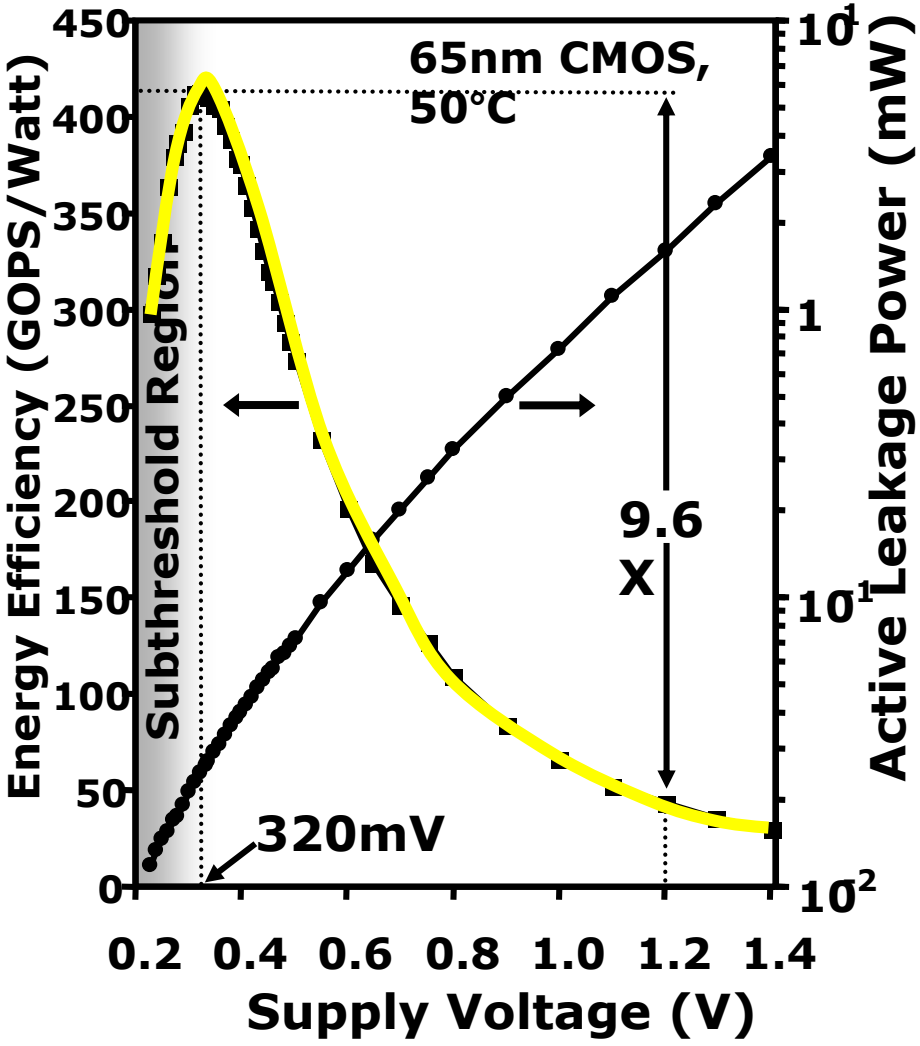
Near Threshold Voltage Operation

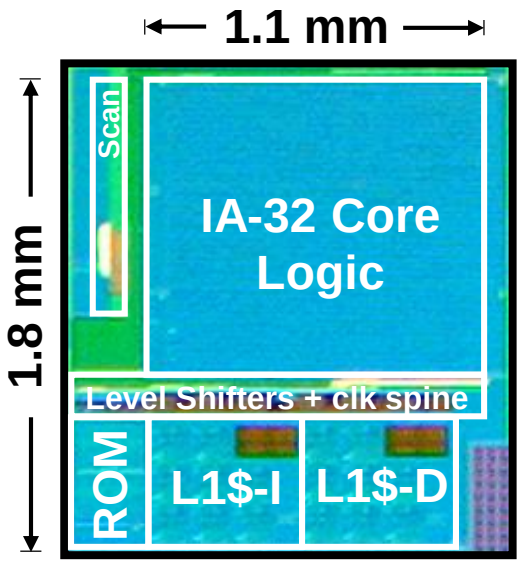




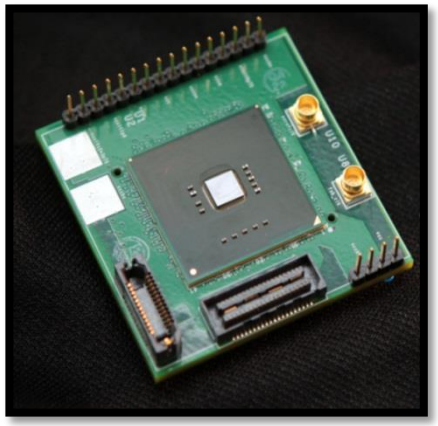
Why wait for TFET's? NTV is here, today!

Ref: H. Kaul et al, "A 320 mV 56 μW 411 GOPS/Watt Ultra-Low Voltage Motion Estimation Accelerator in 65 nm CMOS", JSSC, 2009

Experimental NTV Processor

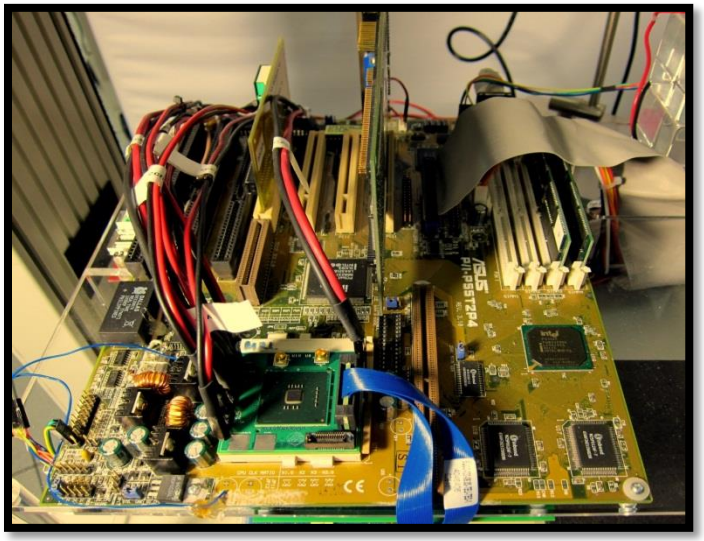


951 Pin FCBGA Package



Custom Interposer

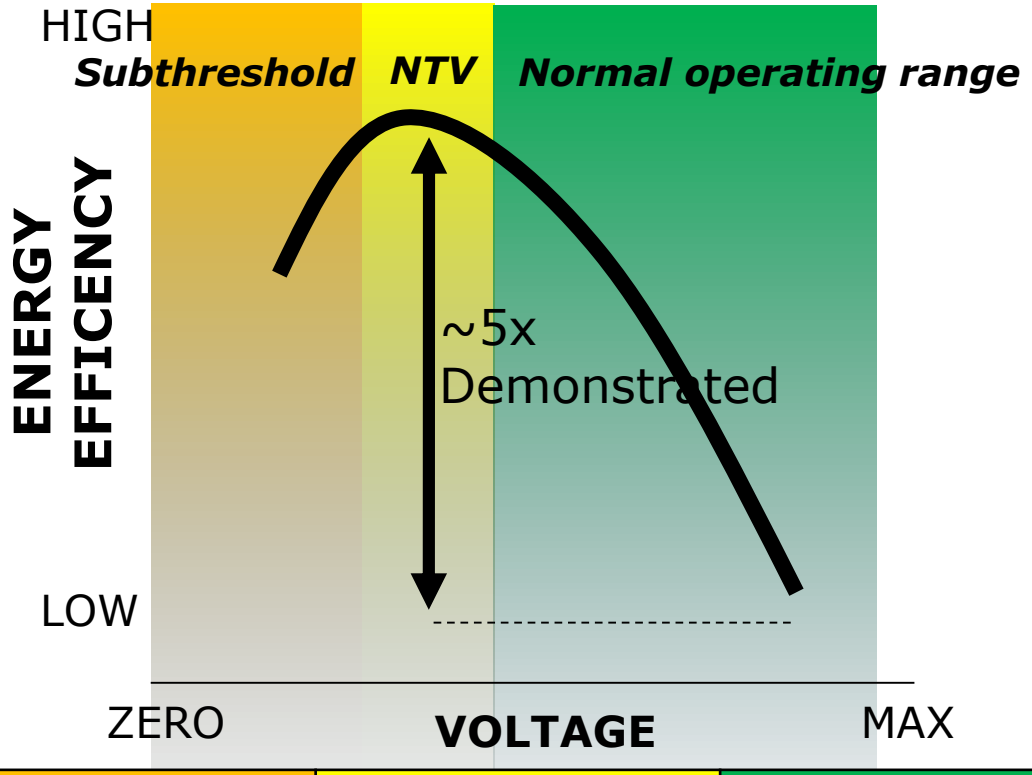
Technology	32nm High-K Metal Gate
Interconnect	1 Poly, 9 Metal (Cu)
Transistors	6 Million (Core)
Core Area	2mm^2



Legacy Socket-7 Motherboard

Ref: S. Jain, et al, "A 280mV-to-1.2V Wide-Operating-Range IA-32 Processor in 32nm CMOS", ISSCC 2012

Wide Dynamic Range



Ultra-low Power	Energy Efficient	High Performance
280 mV	0.45 V	1.2 V
3 MHz	60 MHz	915 MHz
2 mW	10 mW	737 mW
1500 Mips/W	5830 Mips/W	1240 Mips/W

Fine-grain Power Management

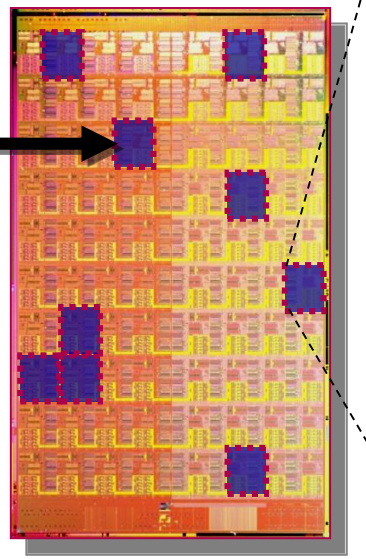
Mode		Power Saving	Wake up
Normal	All active	-	-
Standby	Logic off Memory on	50%	Fast
Sleep	Logic and Memory off	80%	Slow

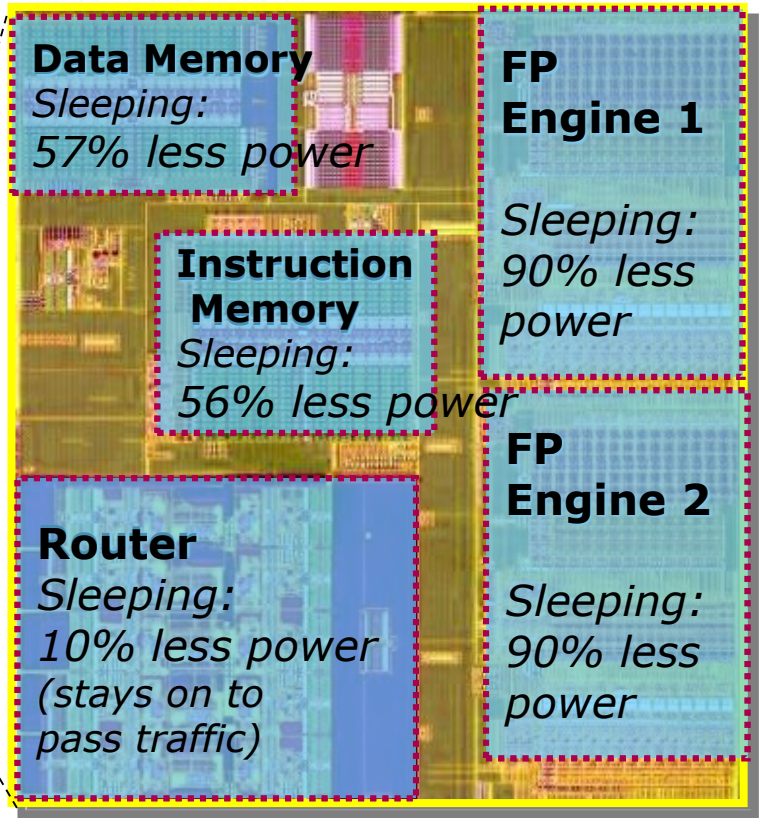
Dynamic, within a core
21 sleep regions per tile *(not all shown)*

Dynamic Chip Level

STANDBY:
- Memory retains data
- **50%** less power/tile

FULL SLEEP:
- Memories fully off
- **80%** less power/tile





Energy efficiency increases by 60%

Ref: Vangal et al, JSSC, January 2008

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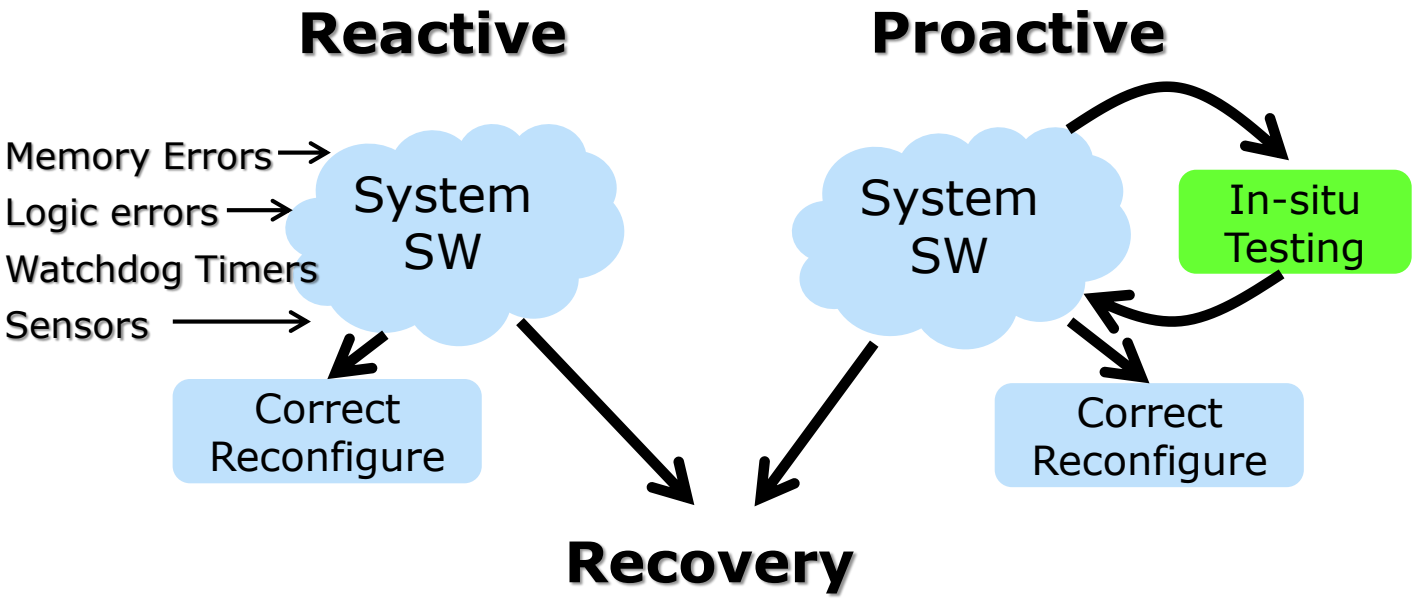
Resiliency—Asymptotic TMR

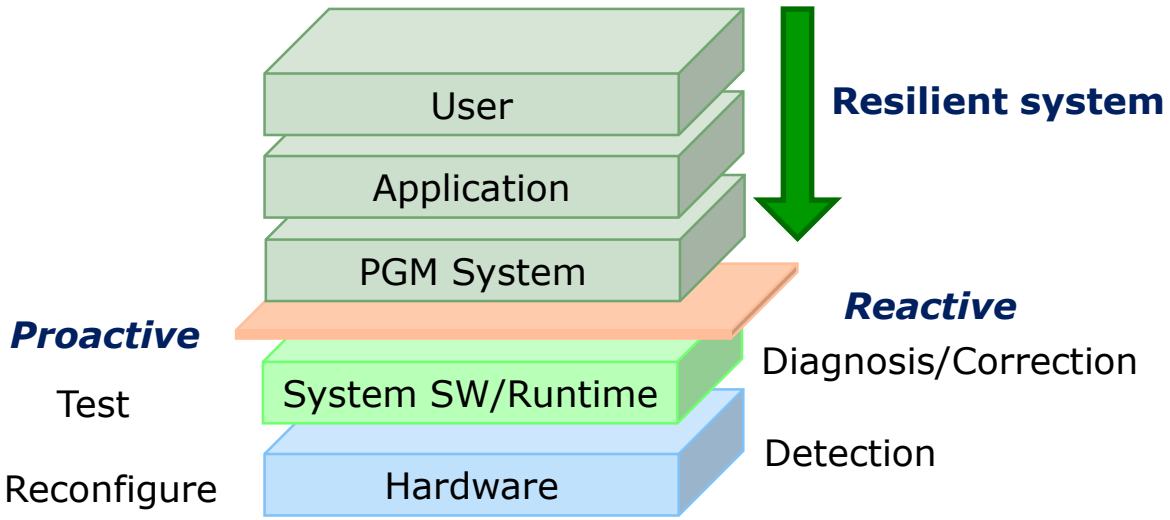
Error detection in HW, correction in SW



Strategy depends on mean time to fault (T)
For large T, traditional check-pointing may be good enough
For small T, incremental, hierarchical check-pointing

❶ System SW, ❷ Test, ❸ Recovery

User Experiences a Reliable System (TMR)



Summary

- **Nothing in (my) sight today to replace CMOS**
- **CMOS must continue until then**
- **Reclaim efficiency, be brave, multi-discipline**
- **Future is bright, we need to:**

Get our heads out of sand…